In the Claims:

1. (Currently Amended) A transistor device comprising:

a semiconductor region having a top surface;

a source region in the semiconductor region;

a drain region in the semiconductor region;

a channel region in the semiconductor region between the source region and the drain region and having a top surface proximate the top surface of the semiconductor region;

an implanted impurity region within and surrounded by the channel region and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region and a second outer boundary proximate, but laterally spaced apart from the drain region;

a gate overlying the channel region; and

a gate dielectric between the gate and the channel region.

2. (Original) The device of claim 1 wherein the semiconductor region comprises a region of monocrystalline silicon.

3. (Original) The device of claim 2 wherein the semiconductor region comprises a silicon substrate.

4. (Currently Amended) The device of claim 1 wherein the source and drain regions extend into the semiconductor region a first distance, and wherein the implanted impurity region is spaced from the top surface by a distance less than the first distance.

5. (Original) The device of claim 1 wherein the gate dielectric comprises silicon dioxide.

6. (Currently Amended) The device of claim 1 wherein the implanted impurity region comprises a region of an implanted oxygen bearing species in the channel region.

7. (Original) The device of claim 1 wherein the channel region comprises a strained channel region.

8. (Original) The device of claim 1 and further comprising:

a first sidewall spacer adjacent a first sidewall of the gate;

a second sidewall spacer adjacent a second sidewall of the gate;

a lightly doped drain region within the semiconductor region adjacent the drain region, the lightly doped drain region disposed beneath the first sidewall; and

a lightly doped source region within the semiconductor region adjacent the source region, the lightly doped source region disposed beneath the second sidewall.

9. (Currently Amended) The device of claim 1 and further comprising a second transistor, the second transistor including:

a second source region in the semiconductor region;

a second drain region in the semiconductor region;

a second channel region in the semiconductor region between the second source region and the second drain region and having a top surface proximate the top surface of the semiconductor region;

a second gate overlying the channel region; and

a second gate dielectric between the gate and the channel region.

10. (Currently Amended) The device of claim 9 further comprising a second implanted impurity region within and surrounded by the second channel region and spaced from the top surface, the second implanted impurity region having a first outer boundary proximate, but laterally spaced apart from the source region and a second outer boundary that is proximate, but laterally spaced apart from the drain region.

11. (Original) The device of claim 9 wherein the second transistor does not include an impurity region within the second channel region.

12. (Original) The device of claim 9 wherein the second transistor device comprises an n-channel transistor.

13.-29. (Canceled)

30. (New) A CMOS device, the CMOS device having a P channel and an N channel transistor, comprising:

a semiconductor region having a top surface;

a first well doped to an N type formed within the semiconductor region and having a top surface proximate the top surface of the semiconductor region, for the P channel transistor;

a P type source region formed in the first well;

a P type drain region formed in the first well;

a channel region formed in the first well in the semiconductor region between the source

region and the drain region and having a top surface proximate the top surface of the semiconductor region;

a first implanted impurity region within and surrounded by the channel region in the first well and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region in the first well and a second outer boundary proximate, but laterally spaced apart from the drain region in the first well;

a gate for the P channel transistor overlying the channel region in the first well;

a gate dielectric between the gate for the P channel transistor and the channel region in the first well;

a second well doped to a P type formed within the semiconductor region and having a top surface proximate the top surface of the semiconductor region, for the N channel transistor;

an N type source region formed in the second well;

an N type drain region formed in the second well;

a channel region formed in the second well in the semiconductor region between the source region and the drain region and having a top surface proximate the top surface of the semiconductor region;

a gate for the N channel transistor overlying the channel region in the second well; and

a gate dielectric between the gate for the N channel transistor and the channel region in the second well.

31. (New) The CMOS device of claim 30 further comprising a second implanted impurity region within and surrounded by the channel region in the second well and spaced from the top surface, the second implanted impurity region having a first outer boundary proximate, but

laterally spaced apart from the source region in the second well and a second outer boundary that is proximate, but laterally spaced apart from the drain region in the second well.

32. (New) The CMOS device of claim 30 wherein the semiconductor region comprises a region of monocrystalline silicon.

33. (New) The CMOS device of claim 30 wherein the semiconductor region comprises a silicon substrate.

34. (New) The CMOS device of claim 30 wherein the first implanted_impurity region comprises a region of an implanted oxygen bearing species in the channel region.

35. (New) The CMOS device of claim 30 wherein the channel region comprises a strained channel region.

36. (New) A CMOS device, comprising:

a semiconductor region having a top surface;

a first well doped to an N type formed within the semiconductor region and having a top surface proximate the top surface of the semiconductor region, for a P channel transistor;

a P type source region formed in the first well;

a P type drain region formed in the first well;

a channel region formed in the first well in the semiconductor region between the source region and the drain region and having a top surface proximate the top surface of the semiconductor region;

a gate for the P channel transistor overlying the channel region in the first well;

a gate dielectric between the gate for the first P channel transistor and the channel region in the first well;

a second well doped to a P type formed within the semiconductor region and having a top surface proximate the top surface of the semiconductor region, for an N-channel transistor;

an N type source region formed in the second well;

an N type drain region formed in the second well;

a channel region formed in the second well in the semiconductor region between the source region and the drain region and having a top surface proximate the top surface of the semiconductor region;

a gate for the second N channel transistor overlying the channel region in the second well;

a gate dielectric between the gate for the N channel transistor and the channel region in the second well; and

at least one implanted impurity region disposed within and surrounded by the channel region in a selected one of the first and the second well and spaced from the top surface, the impurity region having a first outer boundary that is proximate, but laterally spaced apart from the source region in the selected one of the first and the second well and a second outer boundary proximate, but laterally spaced apart from the drain region in the selected one of the first and tehs second well.

37. (New) The device of claim 36 wherein the implanted impurity region comprises a region of an implanted oxygen bearing species in the channel region.